FAIRCHILD SEMICONDUCTOR®

June 2000
Revised October 2006

FSTUD16211
24-Bit Bus Switch with −2V Undershoot Protection and Level Shifting

General Description

The Fairchild Switch FSTUD16211 provides 24-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. A diode to V_{CC} has been integrated into the circuit to allow for level shifting between 5V inputs and 3.3V outputs.

The device is organized as a 12-bit or 24-bit bus switch. When $\overline{OE}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, Port 2A is connected to Port 2B. When $\overline{OE}_{1/2}$ is HIGH, a high impedance state exists between the A and B Ports. The A and B Ports have "undershoot hardened" circuit protection to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit (UHC®) senses undershoot at the I/O's, and responds by preventing voltage differentials from developing and turning on the switch.

Features

- Undershoot hardened to −2V (A and B Ports)
- Voltage level shifting
- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- See Applications Note AN-5008 for details
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

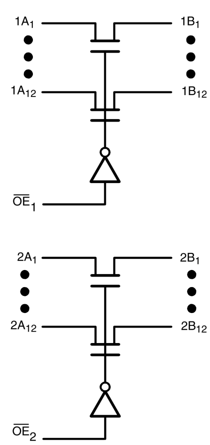
Ordering Code:

Order Number	Package Number	Package Description
FSTUD16211GX (Note 1)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
FSTUD16211MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 1: BGA package available in Tape and Reel only.

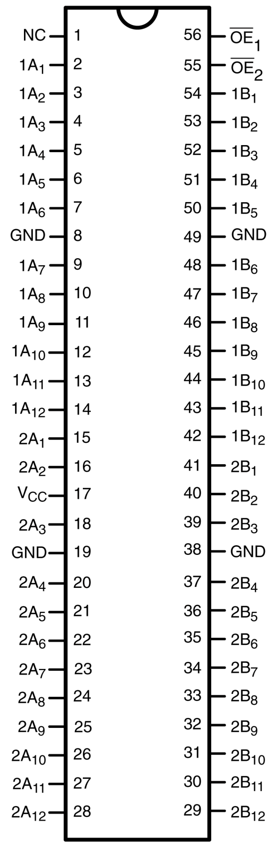
Logic Diagram



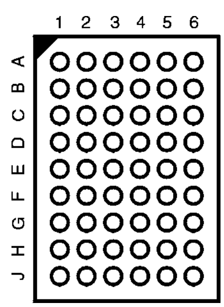
UHC® is a registered trademark of Fairchild Semiconductor Corporation.

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B
NC	No Connect

Pin Assignment for FBGA

	1	2	3	4	5	6
A	$1A_2$	$1A_1$	NC	OE_2	$1B_1$	$1B_2$
B	$1A_4$	$1A_3$	$1A_7$	OE_1	$1B_3$	$1B_4$
C	$1A_6$	$1A_5$	GND	$1B_7$	$1B_5$	$1B_6$
D	$1A_{10}$	$1A_9$	$1A_8$	$1B_8$	$1B_9$	$1B_{10}$
E	$1A_{12}$	$1A_{11}$	$2A_1$	$2B_1$	$1B_{11}$	$1B_{12}$
F	$2A_4$	$2A_3$	$2A_2$	$2B_2$	$2B_3$	$2B_4$
G	$2A_6$	$2A_5$	V_{CC}	GND	$2B_5$	$2B_6$
H	$2A_8$	$2A_7$	$2A_9$	$2B_9$	$2B_7$	$2B_8$
J	$2A_{12}$	$2A_{11}$	$2A_{10}$	$2B_{10}$	$2B_{11}$	$2B_{12}$

Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S) (Note 3)	–2.0V to +7.0V
DC Input Control Pin Voltage (V_{IN})(Note 4)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) $V_{IN} < 0V$	–50 mA
DC Output (I_{OUT})	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100 mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 5)

Power Supply Operating (V_{CC})	4.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0 ns/V to 5 ns/V
Switch I/O	0 ns/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: V_S is the voltage observed/applied at either A or B Ports across the switch.

Note 4: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 5: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C Min	Typ (Note 6)	Max	Units	Conditions
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18 mA
V_{IH}	HIGH Level Input Voltage	4.5–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.5–5.5			0.8	V	
V_{OH}	HIGH Level	4.5–5.5		See Figure 4		V	
I_I	Input Leakage Current	5.5			±1.0	µA	$0 \leq V_{IN} \leq 5.5V$
		0			10	µA	$V_{IN} = 5.5V$
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	$0 \leq A, B \leq V_{CC}$
R_{ON}	Switch On Resistance	4.5		4	7	Ω	$V_{IN} = 0V$, $I_{IN} = 64$ mA
	(Note 7)	4.5		4	7	Ω	$V_{IN} = 0V$, $I_{IN} = 30$ mA
		4.5		35	50	Ω	$V_{IN} = 2.4V$, $I_{IN} = 15$ mA
I_{CC}	Quiescent Supply Current	5.5			1.5	mA	$OE_1 = OE_2$ = GND $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
					10	µA	$OE_1 = OE_2 = V_{CC}$ $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One Input at 3.4V Other Inputs at V_{CC} or GND
V_{IKU}	Voltage Undershoot	5.5			–2.0	V	$0.0 \text{ mA} \geq I_{IN} \geq -50$ mA $\overline{OE}_{1,2} = 5.5V$

Note 6: Typical values are at V_{CC} = 5.0V and T_A= +25°C

Note 7: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\ ^\circ C$ to $+85\ ^\circ C$, $C_L = 50pF$, RU = RD = 500Ω $V_{CC} = 4.5 – 5.5V$		Units	Conditions	Figure No.
		Min	Max			
t_{PHL}, t_{PLH}	Propagation Delay Bus to Bus (Note 8)		0.25	ns	V_I = OPEN	Figures 2, 3
t_{PZH}, t_{PZL}	Output Enable Time	1.5	5.5	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figures 2, 3
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	6.5	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figures 2, 3

Note 8: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 9)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	3.5		pF	V_{CC} = 5.0V
$C_{I/O\ OFF}$	Input/Output Capacitance “OFF State”	5.5		pF	V_{CC} = 5.0V, Switch OFF

Note 9: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 10)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	V_{OH} – 0.3		V	Figure 1

Note 10: This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

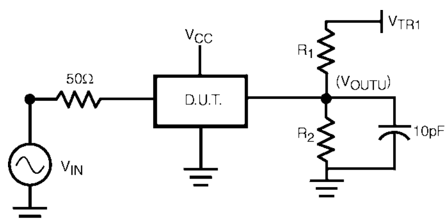
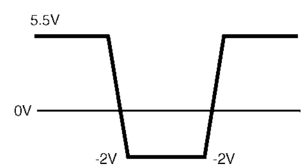


FIGURE 1.

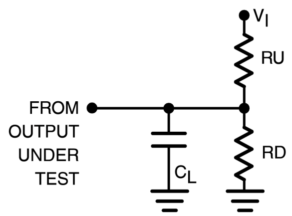
Device Test Conditions

Parameter	Value	Units
V_{IN}	see Waveform	V
$R_1 = R_2$	100K	Ω
V_{TRI}	11.0	V
V_{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: CL includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 2. AC Test Circuit

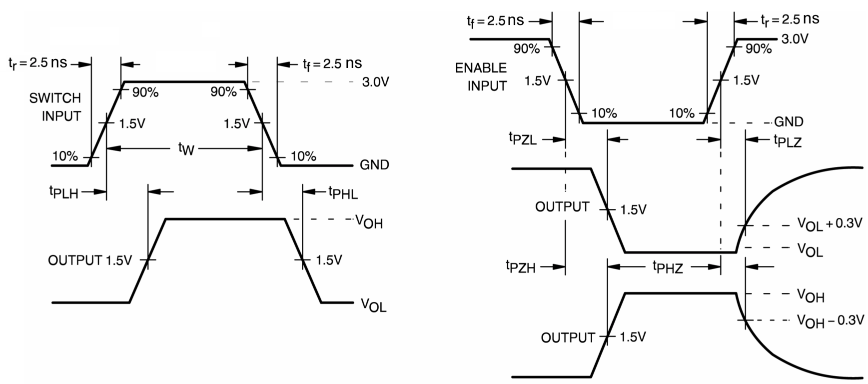


FIGURE 3. AC Waveforms

Output Voltage HIGH vs. Supply Voltage

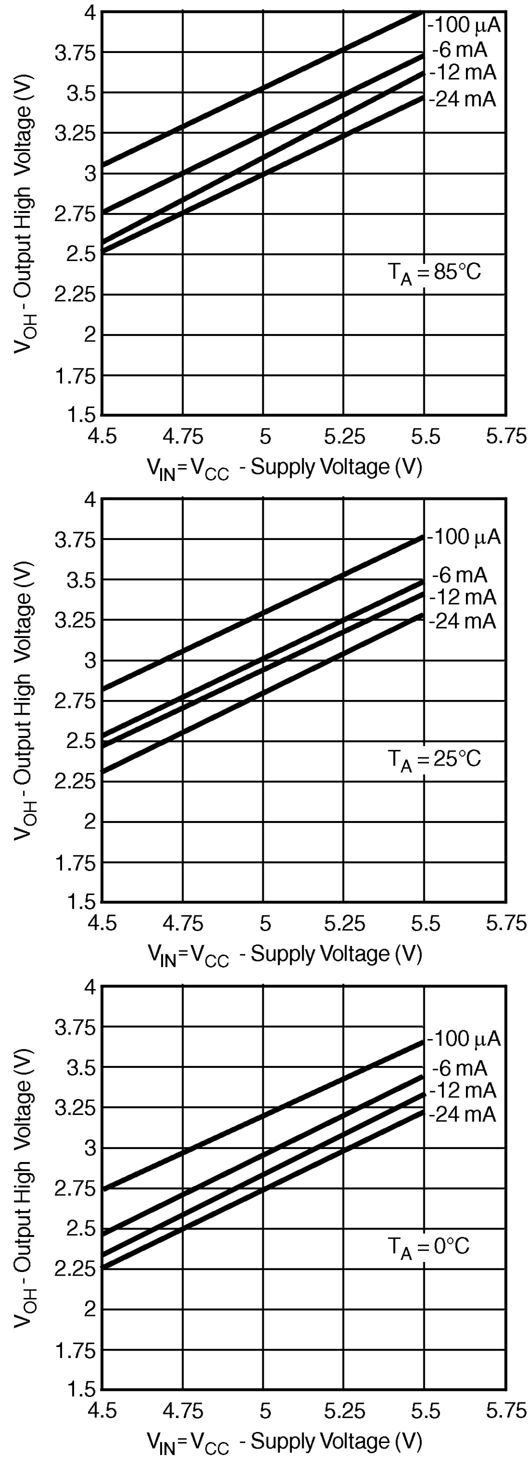
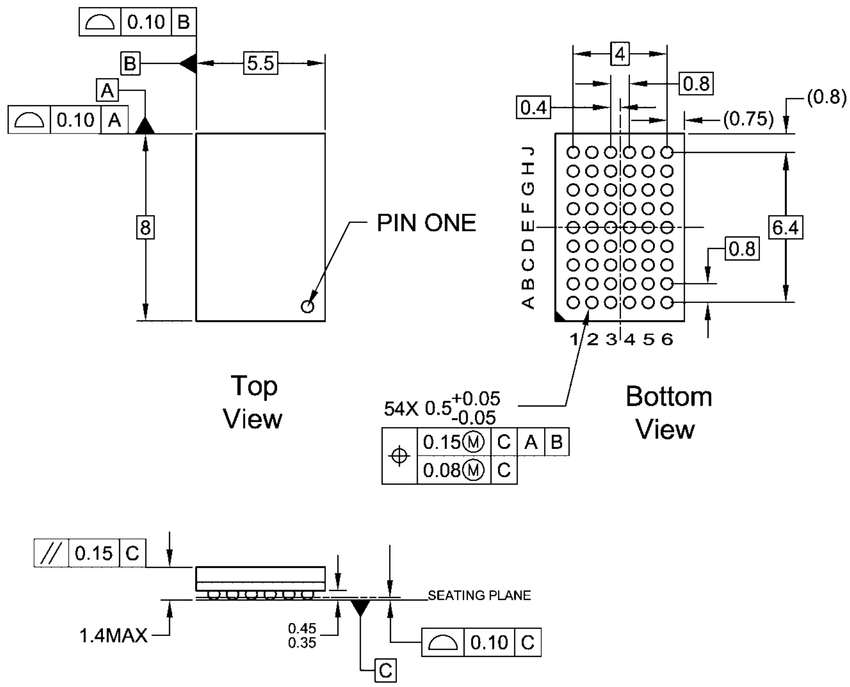


FIGURE 4.

Physical Dimensions inches (millimeters) unless otherwise noted

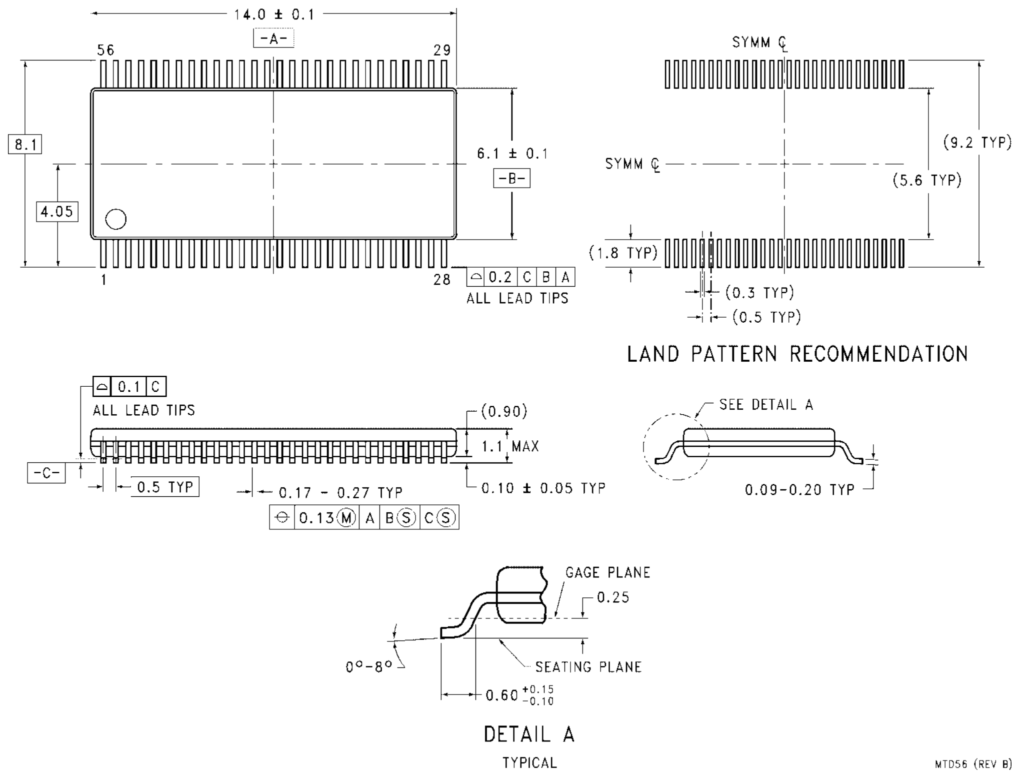


NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
Preliminary

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.